6-6-05

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[2207/12116]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Raj NAIR et al.
Serial No.	:	10/016,793
Filed	:	October 26, 2001
For	:	SILICON INTERPOSER-BASED HYBRID VOLTAGE REGULATOR SYSTEM FOR VLSI DEVICES
Art Unit	:	2838
Examiner	:	Rajnikant B. Patel

Mail Stop PETITION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION TO WITHDRAW A HOLDING OF ABANDONMENT UNDER 37 C.F.R. § 1.181(a)

S I R:

Applicants petition for a withdrawal of the holding of abandonment of the above-identified application.

A Notice of Abandonment of the above-identified application was mailed on May 16, 2005 because Applicant's response to the September 9, 2004 Office Action was either misdirected or otherwise not placed in Applicant's file at the Patent Office.

Applicant's prepared and mailed an Amendment in response to the September 9, 2004 Office Action, including a Request for Three-Month Extension of Time, in the above-identified patent application on March 9, 2005, forwarding the indicated papers via first class mail.

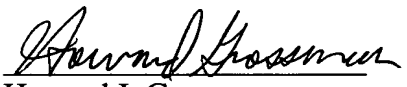
Annexed hereto as Exhibit A is a copy of the Amendment, including a Request for Three-Month Extension of Time, as filed by first class mail on March 9, 2005. The certificate of mailing is properly executed, indicating mailing on March 9, 2005.

Annexed hereto as Exhibit B is a copy of the postcard submitted with the Amendment filed March 9, 2005, stamped received by the United States Patent Office on March 14, 2005.

Accordingly, it is respectfully submitted that the foregoing is a sufficient showing that the Amendment in response to the September 9, 2004 Office Action, including a Request for Three-Month Extension of Time, were submitted in a timely fashion and that the Notice of Abandonment should be withdrawn.

The Commissioner is hereby authorized to charge any fees required in connection with the papers transmitted herewith to Deposit Account No. 11-0600. A duplicate copy of this paper is enclosed for charging purposes.

Respectfully submitted,
KENYON & KENYON

Dated: June 3, 2005 By: 

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Examiner	:	Rajnikant B. Patel
Confirmation No.	:	6063

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

Date: March 9, 2005 Reg. No. 48,673

Signature: Howard Grossman
Howard Grossman

AMENDMENT TRANSMITTAL &
REQUEST FOR THREE-MONTH EXTENSION OF TIME

SIR:

Transmitted herewith for filing in the above-identified patent application is an Amendment in response to the outstanding Office Action dated September 9, 2004. This is also a Petition Under 37 C.F.R. § 1.136(a), for a three-month extension of time to extend the three-month response date of December 9, 2004 by three months from December 9, 2004 to March 9, 2005.

The Commissioner is authorized to charge the appropriate fee, which is believed to be **$1020.00** for the three-month extension, to Kenyon & Kenyon Deposit Account No. **11-0600**, and is also authorized, as appropriate and/or necessary, to charge any additional fees or credit any overpayment to Kenyon & Kenyon Deposit Account No. **11-0600**. A duplicate copy of this transmittal letter is enclosed for these purposes.

Respectfully submitted,

KENYON & KENYON

Dated: March 9, 2005 By: Howard Grossman

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Raj NAIR et al.
Serial No.	:	10/016,793
Filed	:	October 26, 2001
For	:	**SILICON INTERPOSER-BASED HYBRID VOLTAGE REGULATOR SYSTEM FOR VLSI DEVICES**
Art Unit	:	2838
Examiner	:	Rajnikant B. Patel

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

SIR:

In response to the Office Action mailed on September 9, 2004, please reconsider the above-identified application based on the following.

Amendments to the Claims are reflected in the listing of the claims which begins on page 2 of this paper.

Remarks begin on page 6 of this paper.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:
Mail Stop Amendment
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
on

Date: March 9, 2005

Signature: Chandra Seeram

Amendments to the CLAIMS:

Without prejudice, this listing of the claims replaces all prior versions and listings of the claims in the present application:

LISTING OF CLAIMS:

1. (Previously Presented) An apparatus comprising:

a voltage regulation module coupled to an integrated circuit die having an exposed surface layer, the voltage regulation module including:

an interposer layer including voltage regulator elements, the interposer layer having surface dimensions approximately matching the exposed surface layer of the integrated circuit die and being adapted to be stacked surface-to-surface with the exposed surface layer; and

interconnect elements adapted to couple the interposer layer to the integrated circuit die.

2. (Previously Presented) The apparatus of claim 1, wherein the interposer layer is thinned to enable thru-vias to penetrate completely through the interposer.

3. (Previously Presented) The apparatus of claim 1, wherein the voltage regulator elements include both linear regulator elements and switching regulator elements, the linear regulator elements being situated to provide voltage regulation to areas on the integrated circuit die that intermittently demand high current levels.

4. (Previously Presented) The apparatus of claim 3, further comprising:

passive circuit elements, the passive circuit elements including at least one of metal-insulator metal capacitors and high-bandwidth inductors.

5. (Previously Presented) An apparatus comprising:

a voltage regulation module directly coupled to an exposed surface layer of an integrated circuit die including:

a two-dimensional hybrid array of voltage regulator elements, the voltage regulator elements including a minority of linear regulator elements and a majority of switching regulator elements, the two-dimensional array converting a

supply voltage into a regulated voltage and providing the regulated voltage to the integrated circuit die;

wherein the minority of linear regulator elements supply regulated voltage to areas on the integrated circuit die that intermittently demand high current levels.

6. (Previously Presented) The apparatus of claim 5, wherein the two-dimension hybrid array is embedded in an interposer adapted to interface two-dimensionally with the exposed surface layer.

7. (Previously Presented) The apparatus of claim 6, further comprising:

thru-vias penetrating through and insulated from the interposer, the thru-vias being adapted to connect the exposed surface of the integrated circuit die with a substrate.

8. (Previously Presented) The apparatus of claim 6, wherein the hybrid array of voltage regulator elements includes both linear regulator elements and switching regulator elements, the linear regulator elements being situated to interface with and provide voltage regulation to areas on the integrated circuit die that intermittently demand high current levels.

9. (Previously Presented) The apparatus of claim 8, further comprising:

passive circuit elements, the passive circuit elements including at least one of metal-insulator metal capacitors and high-bandwidth inductors.

10. (Currently Amended) A system comprising:

a power supply;

a substrate coupled to the power supply;

an integrated circuit die having an exposed circuit side; and

an interposer situated between the substrate and the integrated circuit die, the interposer having voltage regulator elements for receiving voltage from the power supply and for down-converting the voltage from the power supply into a regulated voltage, the interposer delivering the regulated voltage to the integrated circuit die;

wherein the voltage regulator elements include a minority of linear regulator elements and a majority of switching regulator elements.

11. (Previously Presented) The system of claim 10, wherein the interposer and the exposed circuit side of the integrated circuit die are bonded in a flip-chip fashion.

12. (Previously Presented) The system of claim 11, further comprising:

thru-vias penetrating through and insulated from the interposer, the thru-vias being connecting the exposed circuit side of the integrated circuit die directly to the substrate;

wherein the interposer includes a circuit side coupled to the exposed circuit side of the integrated circuit die with short solder ball elements, and a reverse side coupled to the substrate with interconnect elements.

13. (Currently Amended) The system of claim 11, wherein ~~the interposer includes a hybrid array of voltage regulator elements, the hybrid array of voltage regulator elements including both linear regulator elements and switching regulator elements,~~ the linear regulator elements ~~being~~ are situated to provide voltage regulation to areas on the integrated circuit die that intermittently demand high current levels.

14. (Previously Presented) A method comprising:

coupling an array of distributed low bandwidth and high bandwidth voltage regulators surface-to-surface to an integrated circuit die;

determining locations of hot spots on the integrated circuit die; and

placing the high bandwidth voltage regulators on locations of the array corresponding to the hot spot locations on the integrated circuit die.

15. (Previously Presented) The method of claim 14, further comprising:

minimizing interconnect distances between the voltage regulators and the integrated circuit die.

16. (Previously Presented) The method of claim 15, further comprising:

embedding the array of distributed high bandwidth and low bandwidth voltage regulators in an interposer having a circuit side and a reverse side;

bonding the circuit side of the interposer to the integrated circuit die in a flip-chip fashion; and

coupling the reverse side of the interposer to a substrate coupled to a power supply.

17. (Previously Presented) The method of claim 14, wherein the high bandwidth voltage regulators are linear regulators, and the low bandwidth voltage regulators are switching regulators.

18. (Previously Presented) The method of claim 15, wherein solder ball elements interconnect the interposer and the integrated circuit die.

19. (Previously Presented) The method of claim 15, wherein copper-to-copper interconnects couple the interposer and the integrated circuit die.

20. (Previously Presented) The method of claim 16, further comprising:

coupling the integrated circuit die directly to the substrate with insulated thru-vias passing through the interposer.

REMARKS

Claims 1 to 20 are currently pending in the present application with claims 10 and 13 having been amended herein. The amendments to the claims do not present new matter.

Claims 1, 5 and 14 have been rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,366,467 to Patel et al. (hereinafter "Patel") and by Klughart, U.S. Patent No. 6,396,137 (in paragraph three of the Office Action). It is respectfully submitted that neither Patel nor Klughart anticipates the subject matter of claims 1, 5 and 14 for the following reasons.

As regards the anticipation rejections of the claims, to reject a claim under 35 U.S.C. § 102(e), the Office must demonstrate that each and every claim feature is identically described or contained in a single prior art reference. (See Scripps Clinic & Research Foundation v. Genentech, Inc., 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991))(emphasis added).

Claim 1 recites an interposer layer including voltage regulator elements, the interposer layer having surface dimensions approximately matching the exposed surface layer of the integrated circuit die and being adapted to be stacked **surface-to-surface** with the exposed surface layer.

As regards the Patel reference, the step-down-converter (SDC) and integrated circuit package disclosed therein is precisely the background art referred to in the specification of the above-identified application, which the present invention is intended to improve upon. In particular, Patel discloses placing the SDC, which regulates the voltage, ***adjacent*** to the integrated circuit, both of which are situated on top of an interposer (See Patel, Figure 3 in which the SDC is numbered as (302), the integrated circuit as (304) and the interposer as (306)). Thus, in Patel, the interposer itself does not include voltage regulator elements, but merely includes conductive traces, serving as an electrical conduit. See Patel, col. 3, lines 66-67; col. 4, lines 34-35.

Accordingly, Applicants respectfully submit that Patel does not disclose (or suggest) an interposer layer including voltage regulator elements that is adapted to be stacked **surface-to-surface** with the exposed surface layer. Furthermore, in each of the embodiments disclosed in Patel, the interposer layer is much larger in surface area than the integrated circuit die so that Patel also does not disclose (or suggest) an interposer

layer that has surface dimensions approximately matching the exposed surface layer of the integrated circuit die.

For at least these reasons, it is submitted that Patel does not anticipate the subject matter of claim 1.

As claims 5 and 14 recite features analogous to those of claim 1, it is submitted that Patel also does not anticipate the subject matter of these claims.

With regard to the Klughart reference, as discussed in the previously submitted amendment of July 7, 2004, Klughart does not disclose stacking a voltage regulator layer directly *surface-to-surface* with the exposed surface layer of the integrated circuit die, but rather, explicitly provides for a separate insulating layer (2605 of Figure 17) situated between the voltage regulator/switch and the integrated circuit. Accordingly, in Klughart, the layer that includes a voltage regulator is not stacked surface-to-surface with the exposed layer of the integrated circuit die.

Moreover, the positioning of the insulating layer described in Klughart is not merely a matter of design choice since the silicon-on-insultaor (SOI) fabrication technique used to produce the structure topology in Klughart ***necessarily*** **produces an insulating layer** in between the foundation integrated circuit and a conduction routing layer including a power supply. See Klughart, col. 27, line 62 to col. 28, line 11. Thus, Klughart not only does not disclose a surface-to-surface coupling between a voltage regulator and an integrated circuit but actually plainly teaches away from this structure.

For at least these reasons, Klughart does not anticipate the subject matter of independent claim 1.

As claims 5 and 14 recite features analogous to those of claim 1, it is submitted that Klughart also does not anticipate the subject matter of these claims.

Withdrawal of the anticipation rejection of claims 1, 5 and 14 based on either Patel or Klughart is accordingly respectfully requested.

Claims 10-13 have been rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,521,530 to Peters et al. ("Peters").

Independent claim 10, as amended, recites an interposer having voltage regulator elements that include a minority of linear regulator elements and a majority of switching regulator elements. Peters does not disclose this feature. At most, Peters refers to an interposer that includes "active" elements and capacitors. See Peters, col. 20. There is no specific reference to or suggestion of a voltage regulator having both linear regulator and switching elements, let alone a regulator in which the linear regulator elements

comprise a minority and the switching elements comprise a majority. Accordingly, Peters does not anticipate claim 10 or its dependent claims 11-13.

Claims 2-4, 6-13, and 15-20 have been rejected under 35 U.S.C. § 103(a) as unpatentable over Patel in view of U.S. Patent No. 6,264,475 to Li et al. ("Li"). It is respectfully submitted that the combination of Patel and Li does not render obvious the subject matter of claims 2-4, 6-13 and 15-20.

Establishment of *prima facie* obviousness requires satisfaction of three separate criteria. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

It is submitted that the Li reference fails to cure the deficiencies of the primary Patel reference in that it also does not disclose or suggest an interposer layer including voltage regulator elements having surface dimensions approximately matching the exposed surface layer of the integrated circuit die and being adapted to be stacked surface-to-surface with the exposed surface layer. In contrast, Li merely discloses a resilient interposer that provides improved structural properties but does not include voltage regulator elements.

Accordingly, the combination of Patel and Li fails to disclose or suggest each of the elements of independent claims 1, 5, 10 and 14 and dependent claims 2-4, 6-9, 11-13 and 15-20.

Withdrawal of the obviousness rejection of claims 2-4, 6-13 and 15-20 is accordingly respectfully requested.

Claims 10-13 have been rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,262,905 to Zhang et al. ("Zhang") in view of U.S. Patent No. 6,265,771[1] to Ference et al. ("Ference"). It is respectfully submitted that the combination of Zhang and Ference does not render obvious the subject matter of claims 10-13.

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[1] The Examiner apparently inadvertently referred to the patent number of another cited reference when referring to Ference.

Claim 10 recites an interposer situated between the substrate and the integrated circuit die, the interposer having voltage regulator elements for receiving voltage from the power supply and for down-converting the voltage from the power supply into a regulated voltage. As discussed in the previous response, Ference merely refers to integrating a heat sink into an integrated circuit, and does not mention or refer to an interposer layer including voltage regulator elements as claimed. It is therefore submitted that the combination of Zhang and Ference fails to disclose or suggest each of the elements of independent claim 10 and its dependent claims 11-13.

Withdrawal of the obviousness rejection of claims 10-13 is accordingly respectfully requested.

CONCLUSION

All issues having been addressed, it is believed that the present application is in condition for allowance. Prompt reconsideration and allowance of the present application are respectfully requested.

Respectfully submitted,

KENYON & KENYON

Dated: 3/9/05

By: Howard I. Grossman

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Case No. 22071/2116 Atty. HG

Ser. No. 10/016,793 Due Date 3/9/05

The Impressed Mail Room date stamp acknowledges receipt of the date indicated of:

☐ Application	☒ Extension Request
☒ Amendment	☐ Priority Document
☐ Assignment	☐ Issue Fee
☐ Notice of Appeal	☐ Declaration
☐ Prior Art Statement	☐ Small Entity